AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (amended) A field effect transistor (FET) comprising:

a device channel;

a gate disposed above said device channel;

a doped extension at said each end of said device [[thin]] channel, said doped extension being a source/drain extension; and

portions of a low resistance material layer disposed on said gate and on said source/drain extension, ~~lateral extension contact~~ said portions on each said source/drain extension providing direct contact with said source/drain extension and being lateral extension contact portions, [[gate]] said portions on said gate being separated from said lateral extension contact portions.

2. (original) A FET as in claim 1, wherein each said source/drain extension has a lateral thickness of less than 100Å thick.

3. (original) A FET as in claim 2, wherein said low resistance material layer is a silicide layer.

4. (original) A FET as in claim 3, wherein said device channel is silicon and said source/drain extension is a doped silicon layer.

5. (original) A FET as in claim 4, wherein said gate comprises polysilicon.

6. (original) A FET as in claim 2, wherein said FET is a p-type FET (PFET).

7. (original) A FET as in claim 2, wherein said FET is a n-type FET (NFET).

8. (original) A FET as in claim 2, wherein said FET is one of a plurality of said FETs on a semiconductor substrate, ones of said plurality being p-type FETs (PFETs) and remaining ones being n-type FETs (NFETs).

9. (original) A FET as in claim 8, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate.

10. (original) A FET as in claim 8, wherein said semiconductor substrate is a bulk silicon substrate.

11. (original) A FET as in claim 4, wherein said silicide forms a smooth silicide/silicon interface with said doped epi layer.

12. (original) A FET as in claim 11, wherein smooth silicide/silicon interface has a roughness of less than 100Å.

13. (canceled)

14. (amended) A FET as in claim 3 [[2]], wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi), cobalt (CoSi), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

15. (original) A FET as in claim 14, wherein said silicide is selected from the group of metals consisting of Wsi, NiSi and CoSi.

16. (original) A FET as in claim 2, wherein said low resistance material layer comprises a metal selected from a group of metals consisting of tungsten, cobalt, nickel, titanium, platinum and Erbium.

17. (original) An integrated circuit (IC) including a plurality of field effect transistors (FETs) disposed on a semiconductor substrate, each of said FETs comprising:

a device channel;

a gate disposed above said device channel;

a source/drain extension less than 100Å thick and disposed at said each end of said thin channel; and

a portion of a low resistance material layer forming a smooth interface with and directly contacting a corresponding said source/drain extension.

18. (original) An IC as in claim 17, wherein said low resistance material layer is a silicide layer.

19. (original) An IC as in claim 18, wherein each said device channel is silicon, each said gate is polysilicon and each source/drain extension is doped silicon.

20. (original) An IC as in claim 19, wherein said plurality of FETs comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.

21. (original) An IC as in claim 20, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate.

22. (original) An IC as in claim 20, wherein said semiconductor substrate is a bulk silicon substrate.

23. (original) An IC as in claim 19, wherein smooth silicide/silicon interface has a roughness of less than 100Å, whereby said corresponding source/drain extensions are free from silicide spiking.

24. (canceled)

25. (original) An IC as in claim 18, wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi), cobalt (CoSi), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

26. (original) An IC as in claim 25, wherein said silicide is selected from the group of metals consisting of WSi, NiSi and CoSi.

27. (original) An IC as in claim 17, wherein said low resistance material layer comprises a metal selected from a group of metals consisting of tungsten, cobalt, nickel, titanium, platinum and Erbium.

28 – 40 (canceled).

41. (new) A field effect transistor (FET) comprising:

a silicon device channel;

a gate disposed above said silicon device channel;

a doped silicon extension layer at said each end of said silicon device channel, said doped silicon extension layer being a source/drain extension laterally formed on an angled undercut following a silicon crystal (111) crystallographic plane; and

portions of a low resistance material layer disposed on said gate and on said source/drain extension, lateral extension contact said portions providing direct contact with said source/drain extension, gate said portions on said gate being separated from said lateral extension contact portions.

42. (new) A FET as in claim 41, wherein each said source/drain extension has a lateral thickness of less than 100Å thick.

43. (new) A FET as in claim 42, wherein said low resistance material layer is a silicide layer, said silicide layer being a layer of silicide material selected from a group of materials consisting of a silicide of tungsten (WSi), cobalt (CoSi), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

44. (new) A FET as in claim 42, wherein said gate comprises polysilicon and said FET is one of a plurality of said FETs on a semiconductor substrate, ones of said plurality being p-type FETs (PFETs) and remaining ones being n-type FETs (NFETs).

45. (new) A FET as in claim 44, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate.

46. (new) A FET as in claim 43, wherein said silicide forms a smooth silicide/silicon interface with said doped epi layer.

47. (new) A FET as in claim 46, wherein said smooth silicide/silicon interface has a roughness of less than 100Å.

48. (new) A FET as in claim 43, wherein said silicide is selected from the group of metals consisting of Wsi, NiSi and CoSi.

49. (new) An integrated circuit (IC) including a plurality of field effect transistors (FETs) disposed on a semiconductor substrate, each of said FETs comprising:

a silicon device channel;

a gate disposed above said silicon device channel;

a source/drain extension laterally formed less than 100Å thick on an angled undercut following a silicon crystal (111) crystallographic plane and disposed at said each end of said silicon device channel; and

a portion of a low resistance material layer forming a smooth interface with and directly contacting a corresponding said source/drain extension.

50. (new) An IC as in claim 49, wherein said low resistance material layer is a silicide layer.

51. (new) An IC as in claim 50, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate, each said gate is polysilicon and said plurality of FETs

comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.

52. (new) An IC as in claim 51, wherein said smooth silicide/silicon interface has a roughness of less than 100Å, whereby said corresponding source/drain extensions are free from silicide spiking.

53. (new) An IC as in claim 52, wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi), cobalt (CoSi), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

54. (new) An IC as in claim 53, wherein said silicide is selected from the group of metals consisting of WSi, NiSi and CoSi.

55. (new) An IC as in claim 50, wherein said semiconductor substrate is a bulk silicon substrate, each said gate is polysilicon and said plurality of FETs comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.